and, thus, in view of the forgoing claims 1-60 remain pending for reconsideration which is requested. No new matter has been added. The Examiner's rejections and objections are traversed below.

In the Office Action the Examiner objected to claims 7, 11, 15, 23, 27, 31, 39, 43, 47, 55, 59 and 63 and indicated that these claims would be allowable if rewritten in independent form. These claims have been so rewritten and it is submitted that these claims are now allowable. Withdrawal of the objection is requested.

On page 2 of the Office Action the Examiner rejected claim 1, 4, 6, 17, 20, 22, 33, 36, 38, 49, 52, 54 and 65 under 35 U.S.C. § 102(b) as unpatentable over U.S. Patent No. 5,375,069 Satoh et al.

Satoh is directed to a wiring processing system for designing the wiring routing of a multi-layer interconnection structure for an LSI. In particular, the system automatically assigns gates to cells in accordance with a logic file and a structure library. The system automatically searches for a wiring route between the cells and stores the coordinates in a wiring result file 6 (see figure 1 and col. 5, line 66 - col. 6, line 17). That is, the Satoh system generates coordinate based wiring routes between locations. There is no information associated with the wiring route data that would allow the performance of the wiring to be analyzed.

In contrast, the present invention is designed to produce transmission line data that can be analyzed for performance characteristics such as noise and, as a result, produces "transmission line circuit data suitable for transmission line circuit analysis" (see claims 1, 17, 33 and 49).

It is submitted that the present claimed invention patentably distinguishes over Satoh and withdrawal of the rejection is requested.

Page 3 of the Office Action rejects claims 2, 3, 8-10, 12-14, 16, 18, 19, 24-26, 28-30, 32, 34, 35, 40, 42, 44, 46, 48, 50, 51, 56, 58, 60, 62 and 64 under 35 U.S.C. § 103(a) over U.S. Patent No. 5,046,017 Yuyama et al. in view of U.S. Patent No. 5,375,069 Satoh et al.

Yuyama is directed to a system in which, as depicted in figure 3 and discussed in col. 3, line 50+, the cells are designed, the cell layout is designed and rough wiring is routed. The design with the rough wiring is used to calculate a circuit characteristic that is compared to a target. If the target is not met a re-design occurs starting with the design of the cells. This redesign uses a simple manual process that is added that causes the characteristic to be met.

Satoh as noted above discusses wiring routes being computed and adds nothing to Yuyama

In contrast, in the present invention the logic circuit is "automatically modified when the transmission line circuit is re-edited" (see claims 2, 3, 18, 19, 34, 35, 50, 51), something that the prior art fails to disclose.

It is submitted that the present claimed invention patentably distinguishes over Yuyama and Satoh and withdrawal of the rejection is requested.

The present invention also includes other features not taught or suggested by the prior art. For example, claims 4 and 8 call for the "topology" or shape of the connection to be used in generating the analysis data. The prior art, particularly, Satoh, is only concerned with the physical coordinate connections not with the shape. That is, the invention considers something that the prior art does not. Claims 5, 21, 37, 41, 45, 53, 57 and 61 emphasize that values of passive components (resistors, etc.) are obtained from a table. In the prior art, particularly Satoh, the values are calculated. The present invention operates faster with more consistent values than the prior art. Claim 6, 10, 22, 26, 38, 42, 54 and 58 also emphasize pulling values from a table whereas the prior art of Yuyama does not teach or suggest such.

It is submitted that the invention of the claims distinguishes over the prior art and withdrawal of the rejection is requested.

Respectfully submitted,

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Date: 5/27/03

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By: _____
Date: 5/27/03

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please AMEND the following claims:

1. (Amended) A logical circuit designing device, comprising:

a logical circuit storage unit storing a logical circuit;

a transmission line circuit generation unit generating [a] transmission line circuit data suitable for transmission line circuit analysis based on the logical circuit stored in the logical circuit storage unit; and

a transmission line circuit data storage unit storing the transmission line circuit data generated by the transmission line circuit generation unit.

2. (Amended) A logical circuit designing device, comprising:

a logical circuit storage unit storing a logical circuit;

a transmission line circuit storage unit storing a transmission line circuit corresponding to the logical circuit stored in the logical circuit storage unit;

a transmission line circuit editing unit editing the transmission line circuit stored in the transmission line circuit storage unit; and

a logical circuit modification unit modifying the corresponding logical circuit based on the transmission line circuit edited by the transmission line circuit editing unit, and

wherein the logic circuit is automatically modified when the transmission line circuit is re-edited.

3. (Amended) A logical circuit designing device, comprising:

a logical circuit storage unit storing a logical circuit;

a transmission line circuit generation unit generating a transmission line circuit based on the logical circuit stored in the logical circuit storage unit;

a transmission line circuit storage unit storing the transmission line circuit generated by the transmission line circuit generation unit;

a transmission line circuit editing unit editing the transmission line circuit stored in the transmission line circuit storage unit; and

a logical circuit modification unit modifying the corresponding logical circuit based on the

transmission line circuit edited by the transmission line circuit editing unit, and

wherein the logic circuit is automatically modified when the transmission line circuit is re-edited.

4. The logical circuit designing device according to claim 1, further comprising

a topology designation table storing topology information indicating a type of a connection between active components composing a logical circuit, and

wherein said transmission line circuit generation unit generates a transmission line circuit based on the topology information stored in the topology designation table.

5. The logical circuit designing device according to claim 1, further comprising

a value designation table storing a value of a passive component composing a logical circuit, and

wherein said transmission line circuit generation unit generates a transmission line circuit based on the value stored in the value designation table.

6. The logical circuit designing device according to claim 1, further comprising

an addition designation table storing addition information of a passive component composing a logical circuit, and

wherein said transmission line circuit generation unit generates a transmission line circuit by adding the passive component based on the passive component addition information stored in the addition designation table.

7. (Amended) A logical circuit designing device, comprising: [The logical circuit designing device according to claim 1, further comprising]

a logical circuit storage unit storing a logical circuit;

a transmission line circuit generation unit generating a transmission line circuit based on the logical circuit stored in the logical circuit storage unit;

a transmission line circuit storage unit storing the transmission line circuit generated by the transmission line circuit generation unit; and

a deletion designation table storing deletion information of a passive component composing a logical circuit, and

wherein said transmission line circuit generation unit generates a transmission line circuit

by deleting the passive component based on the passive component deletion information stored in the deletion designation table.

8. The logical circuit designing device according to claim 3, further comprising

a topology designation table storing topology information indicating a type of a connection between active components composing a logical circuit, and

wherein said transmission line circuit generation unit generates a transmission line circuit based on the topology information stored in the topology designation table.

9. The logical circuit designing device according to claim 3, further comprising

a value designation table storing a value of a passive component composing a logical circuit, and wherein said transmission line circuit generation unit generates a transmission line circuit based on the value stored in the value designation table.

10. The logical circuit designing device according to claim 3, further comprising

an addition designation table storing addition information of a passive component composing a logical circuit, and wherein said transmission line circuit generation unit generates a transmission line circuit by adding the passive component based on the passive component addition information stored in the addition designation table.

11. (Amended) A logical circuit designing device, comprising: [The logical circuit designing device according to claim 3, further comprising]

a logical circuit storage unit storing a logical circuit;

a transmission line circuit generation unit generating a transmission line circuit based on the logical circuit stored in the logical circuit storage unit;

a transmission line circuit storage unit storing the transmission line circuit generated by the transmission line circuit generation unit;

a transmission line circuit editing unit editing the transmission line circuit stored in the transmission line circuit storage unit;

a logical circuit modification unit modifying the corresponding logical circuit based on the transmission line circuit edited by the transmission line circuit editing unit; and

a deletion designation table storing deletion information of a passive component composing a logical circuit, and wherein said transmission line circuit generation unit generates

a transmission line circuit by deleting the passive component based on the passive component deletion information stored in the deletion designation table.

12. The logical circuit designing device according to claim 2, wherein said logical circuit modification unit modifies the logical circuit stored in the logical circuit storage unit based on the transmission line circuit edited by the transmission line circuit editing unit.

13. The logical circuit designing device according to claim 9, wherein said logical circuit modification unit modifies the value of a passive component of the logical circuit stored in the logical circuit storage unit based on the transmission line circuit edited by the transmission line circuit editing unit.

14. The logical circuit designing device according to claim 10, wherein said logical circuit modification unit modifies the passive component addition information of the logical circuit stored in the logical circuit storage unit based on the transmission line circuit edited by the transmission line circuit editing unit.

15. The logical circuit designing device according to claim 11, wherein said logical circuit modification unit modifies the passive component deletion information of the logical circuit stored in the logical circuit storage unit based on the transmission line circuit edited by the transmission line circuit editing unit.

16. The logical circuit designing device according to claim 12, wherein said logical circuit modification unit modifies the logical circuit based on a difference between the transmission line circuit edited by the transmission line circuit editing unit and the logical circuit stored in the logical circuit storage unit.

17. (Amended) A logical circuit designing method, comprising:

generating [a] transmission line circuit <u>data suitable for transmission line circuit analysis</u> based on a logical circuit stored in a logical circuit database; and

storing the generated transmission line circuit <u>data</u> in a transmission line circuit database.

18. (Amended) A logical circuit designing method, comprising:

editing the transmission line circuit stored in the transmission line circuit database; and

modifying a logical circuit corresponding to the transmission line circuit based on the edited transmission line circuit, and

wherein the logic circuit is automatically modified when the transmission line circuit is re-edited.

19. (Amended) A logical circuit designing method, comprising:

generating a transmission line circuit based on a logical circuit stored in a logical circuit database;

storing the generated transmission line circuit in a transmission line circuit database

editing the transmission line circuit stored in the transmission line circuit database; and

modifying the generated logical circuit based on the edited transmission line circuit, and

wherein the logic circuit is automatically modified when the transmission line circuit is re-edited.

20. The logical circuit designing method according to claim 17, wherein the transmission line circuit is generated based on topology information stored in a topology designation table storing topology information indicating a type of a connection between active components composing a logical circuit, in said generating.

21. The logical circuit designing method according to claim 17, wherein the transmission line circuit is generated based on a value of a passive component stored in a value designation table storing values of passive components composing a logical circuit, in said generating.

22. The logical circuit designing method according to claim 17, wherein the transmission line circuit is generated by adding a passive component based on passive component addition information stored in an addition designation table storing addition information of passive components composing a logical circuit, in said generating.

23. (Amended) A logical circuit designing method, comprising: [The logical circuit designing method according to claim 17,]

generating a transmission line circuit based on a logical circuit stored in a logical circuit database; and

storing the generated transmission line circuit in a transmission line circuit database, and

wherein the transmission line circuit is generated by deleting a passive component based on passive component deletion information stored in a deletion designation table storing deletion information of passive components composing a logical circuit, in said generating.

24. The logical circuit designing method according to claim 19, wherein the transmission line circuit is generated based on topology information stored in a topology designation table storing topology information indicating a type of a connection between active components composing a logical circuit, in said generating.

25. The logical circuit designing method according to claim 19, wherein the transmission line circuit is generated based on a value stored in a value designation table storing values of passive components composing a logical circuit, in said generating.

26. The logical circuit designing method according to claim 19, wherein the transmission line circuit is generated by adding a passive component based on addition information of the passive component stored in an addition designation table storing addition information of passive components composing a logical circuit, in said generating.

27. (Amended) A logical circuit designing method, comprising: [The logical circuit designing method according to claim 19,]

generating a transmission line circuit based on a logical circuit stored in a logical circuit database;

storing the generated transmission line circuit in a transmission line circuit database

editing the transmission line circuit stored in the transmission line circuit database; and

modifying the generated logical circuit based on the edited transmission line circuit, and

wherein the transmission line circuit is generated by deleting a passive component based on deletion information of the passive component stored in a deletion designation table storing deletion information of passive components composing a logical circuit, in said generating.

28. The logical circuit designing method according to claim 18, wherein the logical

circuit is modified based on the transmission line circuit edited by said editing, in said modifying.

29. The logical circuit designing method according to claim 25, wherein the logical circuit is modified by modifying a value of a logical circuit stored in said logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

30. The logical circuit designing method according to claim 26, wherein the logical circuit is modified by modifying passive component addition information of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

31. The logical circuit designing method according to claim 27, wherein the logical circuit is modified by modifying passive component deletion information of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

32. The logical circuit designing method according to claim 28, wherein the logical circuit is modified based on a difference between a transmission line circuit by edited by said editing and a logical circuit stored in the logical circuit database, in said modifying.

33. (Amended) A computer-readable storage medium which stores a logical circuit designing program for enabling a computer, comprising:

generating [a] transmission line circuit <u>data suitable for transmission line circuit analysis</u> based on a logical circuit stored in a logical circuit database; and

storing the generated transmission line circuit <u>data</u> in a transmission line circuit database.

34. (Amended) A computer-readable storage medium which stores a logical circuit designing program for enabling a computer, comprising:

editing the transmission line circuit stored in the transmission line circuit database; and

modifying a logical circuit corresponding to the transmission line circuit based on the edited transmission line circuit<u>, and</u>

<u>wherein the logic circuit is automatically modified when the transmission line circuit is re-</u>

edited.

35. (Amended) A computer-readable storage medium which stores a logical circuit designing program for enabling a computer, comprising:

generating a transmission line circuit based on a logical circuit stored in a logical circuit database;

storing the generated transmission line circuit in a transmission line circuit database;

editing the transmission line circuit stored in the transmission line circuit database; and

modifying a logical circuit corresponding to the transmission line circuit based on the edited transmission line circuit, and

wherein the logic circuit is automatically modified when the transmission line circuit is re-edited.

36. The storage medium according to claim 33, wherein the transmission line circuit is generated based on topology information stored in a topology designation table that stores topology information indicating types of connections between active components composing a logical circuit, in said generating.

37. The storage medium according to claim 33, wherein the transmission line circuit is generated based on a value stored in a value designation table storing values of passive components composing a logical circuit, in said generating.

38. The storage medium according to claim 33, wherein the transmission line circuit is generated by adding a passive component based on passive component addition information stored in an addition designation table storing addition information of passive components composing a logical circuit, in said generating.

39. (Amended) A computer-readable storage medium which stores a logical circuit designing program for enabling a computer, comprising: [The storage medium according to claim 33,]

generating a transmission line circuit based on a logical circuit stored in a logical circuit database; and

storing the generated transmission line circuit in a transmission line circuit database, and

wherein the transmission line circuit is generated by deleting a passive component based on passive component addition information stored in an addition designation table storing deletion information of passive components composing a logical circuit, in said generating.

40. The storage medium according to claim 35, wherein the transmission line circuit is generated based on topology information stored in a topology designation table storing types of connections between active components composing a logical circuit, in said generating.

41. The storage medium according to claim 35, wherein the transmission line circuit is generated based on a value stored in a value designation table storing values of passive components composing a logical circuit, in said generating.

42. The storage medium according to claim 35, wherein the transmission line circuit is generated by adding a passive component based on passive component addition information stored in an addition designation table storing addition information pf passive components composing a logical circuit, in said generating.

43. (Amended) A computer-readable storage medium which stores a logical circuit designing program for enabling a computer, comprising: [The storage medium according to claim 35,]

generating a transmission line circuit based on a logical circuit stored in a logical circuit database;

storing the generated transmission line circuit in a transmission line circuit database;

editing the transmission line circuit stored in the transmission line circuit database; and

modifying a logical circuit corresponding to the transmission line circuit based on the edited transmission line circuit, and

wherein the transmission line circuit is generated by deleting a passive component based on passive component addition information stored in an addition designation table storing deletion information of passive components composing a logical circuit, in said generating.

44. The storage medium according to claim 34, wherein the logical circuit is modified based on the transmission line circuit edited by said editing, in said modifying.

45. The storage medium according to claim 41, wherein the logical circuit is modified by modifying a value of a logical circuit stored in said logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

46. The storage medium according to claim 42, wherein the logical circuit is modified by modifying passive component addition information of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

47. The storage medium according to claim 43, wherein the logical circuit is modified by modifying passive component deletion information of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

48. The storage medium according to claim 44, wherein the logical circuit is modified based on a difference between a transmission line circuit by edited by said editing and a logical circuit stored in the logical circuit database, in said modifying.

49. (Amended) A logical circuit designing program for enabling a computer, comprising:

generating [a] transmission line circuit <u>data suitable for transmission line circuit analysis</u> based on a logical circuit stored in a logical circuit database; and

storing the generated transmission line circuit <u>data</u> in a transmission line circuit database.

50. (Amended) A logical circuit designing program for enabling a computer, comprising:

editing the transmission line circuit stored in the transmission line circuit database; and

modifying a logical circuit corresponding to the transmission line circuit based on the edited transmission line circuit<u>, and</u>

<u>wherein the logic circuit is automatically modified when the transmission line circuit is re-edited</u>.

51. (Amended) A logical circuit designing program for enabling a computer, comprising:

generating a transmission line circuit based on a logical circuit stored in a logical circuit database;

storing the generated transmission line circuit in a transmission line circuit database;

editing the transmission line circuit stored in the transmission line circuit database; and

modifying a logical circuit corresponding to the transmission line circuit based on the edited transmission line circuit, and

wherein the logic circuit is automatically modified when the transmission line circuit is re-edited.

52. The logical circuit designing program according to claim 49, wherein the transmission line circuit is generated based on topology information stored in a topology designation table that stores topology information indicating types of connections between active components composing a logical circuit, in said generating.

53. The logical circuit designing program according to claim 49, wherein the transmission line circuit is generated based on a value stored in a value designation table storing values of passive components composing a logical circuit, in said generating.

54. The logical circuit designing program according to claim 49, wherein the transmission line circuit is generated by adding a passive component based on passive component addition information stored in an addition designation table storing addition information of passive components composing a logical circuit, in said generating.

55. (Amended) A logical circuit designing program for enabling a computer, comprising: [The logical circuit designing program according to claim 49,]

generating a transmission line circuit based on a logical circuit stored in a logical circuit database; and

storing the generated transmission line circuit in a transmission line circuit database, and

wherein the transmission line circuit is generated by deleting a passive component based on passive component addition information stored in an addition designation table storing deletion information of passive components composing a logical circuit, in said generating.

56. The logical circuit designing program according to claim 51, wherein the

transmission line circuit is generated based on topology information stored in a topology designation table storing types of connections between active components composing a logical circuit, in said generating.

57. The logical circuit designing program according to claim 51, wherein the transmission line circuit is generated based on a value stored in a value designation table storing values of passive components composing a logical circuit, in said generating.

58. The logical circuit designing program according to claim 51, wherein the transmission line circuit is generated by adding a passive component based on passive component addition information stored in an addition designation table storing addition information of passive components composing a logical circuit, in said generating.

59. (Amended) A logical circuit designing program for enabling a computer, comprising: [The logical circuit designing program according to claim 51,]

generating a transmission line circuit based on a logical circuit stored in a logical circuit database;

storing the generated transmission line circuit in a transmission line circuit database;

editing the transmission line circuit stored in the transmission line circuit database; and

modifying a logical circuit corresponding to the transmission line circuit based on the edited transmission line circuit, and

wherein the transmission line circuit is generated by deleting a passive component based on passive component addition information stored in an addition designation table storing deletion information of passive components composing a logical circuit, in said generating.

60. The logical circuit designing program according to claim 50, wherein the logical circuit is modified based on the transmission line circuit edited by said editing, in said modifying.

61. The logical circuit designing program according to claim 57, wherein the logical circuit is modified by modifying a value of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

62. The logical circuit designing program according to claim 58, wherein the logical

circuit is modified by modifying passive component addition information of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

63. The logical circuit designing program according to claim 59, wherein the logical circuit is modified by modifying passive component deletion information of a logical circuit stored in the logical circuit database based on the transmission line circuit edited by said editing, in said modifying.

64. The logical circuit designing program according to claim 60, wherein the logical circuit is modified based on a difference between a transmission line circuit by edited by said editing and a logical circuit stored in the logical circuit database, in said modifying.

65. (Amended) A logical circuit designing device, comprising:

logical circuit storage means for storing a logical circuit;

transmission line circuit generation means for generating [a] transmission line circuit <u>data suitable for transmission line circuit analysis</u> based on the logical circuit stored in the logical circuit storage means; and

transmission line circuit storage means for storing the transmission line circuit <u>data</u> generated by the transmission line circuit generation means.